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(54) Method and apparatus for converting an interlace-scan video signal into a non-interlace scan video signal

Verfahren und Vorrichtung zur Umwandlung von Videosignal mit Zeilensprungabtastung in ein Videosignal mit fortlaufender Abtastung

Méthode et dispositif de conversion de signal vidéo à balayage entrelacé en signal vidéo à balayage non-entrelacé

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- **PATENT ABSTRACTS OF JAPAN vol. 009, no. 019 (E-292), 25 January 1985 (1985-01-25) & JP 59 167184 A (SONY KK), 20 September 1984 (1984-09-20)**
- **PATENT ABSTRACTS OF JAPAN vol. 011, no. 081 (E-488), 12 March 1987 (1987-03-12) & JP 61 234194 A (HITACHI LTD;OTHERS: 01), 18 October 1986 (1986-10-18)**

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Description

FIELD OF THE INVENTION

[0001] This invention relates to television receivers and more particularly to television receivers which display interlace-scan video signal as non-interlaced or progressive-scan video images.

BACKGROUND OF THE INVENTION

[0002] Television signals formatted according to all of the major broadcasts standards are interlace-scan video signals. In an interlace-scan video signal, an image frame is displayed as two interleaved fields. One field, the upper field, contains the odd lines of the image frame while the other field, the lower field, contains the even lines of the image frame. Typically, the image fields occur at different times. For example, video signals formatted according to the NTSC standard have a field interval of 1/60 of a second between successive fields.

[0003] It has been known for some time that the display of interlace-scan video images produces artifacts in the displayed images. The most noticeable of these is a vertical dot crawl in which the image picture elements (pixels) which make up vertical lines in the displayed image appear be moving toward the top of the image.

[0004] It has also been known that distortion of this type may be removed if the interlace-scan image is displayed in a non-interlace format. One method of generating a non-interlace-scan image from a interlace-scan signal is to double each line of the interlace-scan signal or to interpolate between successive lines in a field in order to convert individual image fields into image frames. Systems which double lines in order to generate these image frames, tend to have artifacts such as jagged diagonal lines and horizontal lines which oscillate up and down from field to field. The systems which interpolate the intervening lines and image fields have alternating lines of different horizontal resolution, since the horizontal resolution of the interpolated lines is one-half the resolution of the non interpolated lines. Moreover, the relative position of the high resolution and low resolution image lines changes from frame to frame causing additional artifacts.

[0005] Other interlace-scan to progressive-scan conversion systems attempt to generate additional lines in one image field from the other image field which makes up the image frame. These systems use either an adaptive filter method or a linear filter method. The adaptive methods tend to be tricked by noise in the signal. This noise in the image signal may cause the adaptive filter to make the wrong decision, which may result in visible artifacts. Systems employing conventional linear filters have the problem of different frequency responses for pixels in the one image field versus pixels in the other image field or for interpolated versus non-interpolated pixels.

[0006] European Patent no. 0 152 738 A concerns an interlace-to-progressive scan video conversion circuit. The conversion circuit interpolates an interlaced television signal by means of a temporal and spatial filter, to obtain the correct number of output lines, and time compressing the result, to obtain the correct output rate for the generated lines. The disclosed circuit interpolates all frequencies of the luminance signal by averaging samples from the current field with corresponding samples from the previous field.

[0007] Japanese Patent no. 59 167184 A relates to an interlace-to-progressive scan video conversion circuit that corrects "flicker" in luminance of a television signal by averaging video signals from a previous field with video signals from the current field to form the progressive scan signal.

[0008] U.S. Patent no. 5,012,326 concerns an interlace-to-progressive scan video conversion system. The non-interlaced television signal is separated into high and low frequency components. A complex adaptive interpolation filter is used to generate interpolated high-frequency luminance components and low-frequency luminance components. The interpolated low frequency luminance components are a motion-adaptive combination of 1) an average of the current sample and a corresponding frame delayed sample and 2) an average of two vertically adjacent samples delayed by one field interval from the current sample. The interpolated low frequency components are an average of corresponding samples from the current field and the previous field

[0009] Japanese Patent no. 61 234194 appears to describe a color television signal processing system, wherein a color television signal is separated into a luminance signal and first and second color signals. The luminance signal is further separated into high and low frequency components. The low frequency component is of the current field, delayed by one-half line interval or the corresponding sample from the previous field is combined with the high frequency component of the luminance signal to generate a sample of the output video signal. As no speedup memories or interpolation circuits are described, this appears to be a video compression circuit that converts an interlace-scan video signal into an interlace scan video signal in a different format.

[0010] International patent application no. WO 97 13376 concerns an interlace-to progressive scan video conversion system, in which the luminance and chrominance signals are applied to respective interlace to progressive converters that interpolate between vertical samples in a single field to generate the interstitial samples used in the progressive signal. The system includes a vertical bandwidth expander that applies a peaking function vertically to enhance horizontal edges in the image.

[0011] International patent application no. WO 95 19684 relates to a multimode interpolation filter that is used to decompressed MPEG video signals that are in

4:2:0 format into signals in 4:2:2 format. Specifically, an interlaced television signal is divided into chrominance and luminance components, which are then time delayed and recombined to produced an interlace scan video signal having a higher scan rate.

SUMMARY OF THE INVENTION

[0012] The present invention is embodied in an interlace-scan to progressive-scan conversion system, as defined in claim 1, which generates image frames that have a temporal position which is between the temporal positions of the two constituent image fields. The system interpolates image lines for the progressive frames by successively averaging a current line from a current field with the line in the previous field that is immediately above the current line and the line in the previous field which is immediately below the current line when the two fields are displayed.

[0013] According to one aspect of the invention, the interpolation method, as defined in claim 6, is applied only to relatively low-frequency components of the luminance signal information. Higher frequency luminance information is selected from one of the two constituent fields and displayed either by line doubling or after it has been processed by a weighted line interpolation filter.

[0014] According to another aspect of the invention, the low pass filtering used to separate the lower frequency luminance components from the composite video signal is part of the luminance/chrominance separation filter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015]

Figure 1A is a block diagram of video signal processing circuitry which includes an embodiment of the invention.

Figure 1B is a block diagram of a video signal line interpolation circuit suitable for use in the circuitry shown in Figure 1A.

Figure 1C is a block diagram of clock signal generation circuitry suitable for use with the video signal processing circuitry shown in Figures 1A and 1B.

Figure 2A is a video image diagram which illustrates the spatial relationship between two fields that constitute an image frame.

Figure 2B is a vertical-temporal diagram which shows several lines of several video image fields and is useful for describing the environment in which the invention operates.

Figure 2C is a vertical-temporal diagram of several lines of several image fields which is useful for describing the operation of the circuitry as shown in Figure 1B.

Figure 2D is a vertical-temporal diagram of several lines of several fields of an interlaced signal superimposed upon the resulting non-interlaced lines of several frames produced using the circuitry shown in Figure 1B.

Figure 2E is a vertical-temporal diagram showing several lines of several non-interlaced frames produced by the circuitry shown in Figure 1B.

Figure 3 is a graph of vertical sample number versus amplitude for the non-interlaced video signal shown in Figure 2D.

Figure 4 is a graph of sample rate versus amplitude for the non-interlaced video signal shown in Figure 2D.

Figure 5 is a graph of sample rate versus amplitude which is useful for describing the relationship between the filtering provided by a video camera and the embodiment of the invention shown in Figure 1B.

Figure 6 is a block diagram of video signal processing circuitry according to an alternative embodiment of the invention which includes a line interpolator such as that shown in Figure 1B.

Figure 7 is a block diagram of a line repeat circuit suitable for use in the circuitry shown in Figure 6.

Figure 8 is a block diagram of a line comb filter suitable for use in place of the line repeat circuit shown in Figure 6.

DETAILED DESCRIPTION

[0016] Under the standard developed by the National Television Standards Committee (NTSC), video signals are displayed as successive image frames, each frame including two interlaced image fields, an upper field and a lower field. An NTSC frame interval is 1/30 of a second and is divided into two field intervals of 1/60 of a second each. An image frame includes 525 horizontal line intervals divided such that 262 1/2 horizontal lines occur in each image field.

[0017] Figure 2A is an image scan diagram which illustrates the relative spatial position of the two fields of an NTSC video frame. In the reproduced image, the lines 212 of the upper video field are scanned between respective lines 210 of the lower video field.

[0018] The exemplary embodiments of the invention described below, interpolate lines between respective

lines of the two fields to produce lines of an image frame which occupy spatial positions between the lines 210 of the lower field and the lines 212 of the upper field. To generate four lines which are positioned between line 212A and line 212C, for example, line 210A is separately averaged with line 212A and line 212B and line 210B is separately averaged with lines 212B and line 212C. These operations produce interpolated lines of a non-interlaced image frame which have spatial and temporal positions between the lines of the image fields which are used to generate the frames.

[0019] Figure 1A is a block diagram of signal processing circuitry which includes an embodiment of the present invention. In Figure 1A, an interlaced video signal is received and applied to a luminance-chrominance separation circuit 102. The circuit 102 may include, for example, a line comb filter (not shown) which provides luminance and chrominance signals at a sample frequency, $4f_{sc}$, of four times the frequency of the color subcarrier signal. The chrominance signal is a sequence of samples (R-Y), (B-Y), -(R-Y), -(B-Y), (R-Y), ..., where (R-Y) and (B-Y) are color difference signals. The luminance signal provided by the circuit 102 has a bandwidth of approximately 4 MHz while the chrominance signal has a bandwidth of approximately 0.5 MHz.

[0020] The luminance signal provided by the luminance-chrominance separation circuit 102 is applied to a line interpolator 106 according to the present invention. An exemplary circuit suitable for use as the line interpolator 106 is described below with reference to Figure 1B. As described below, the line interpolator provides luminance samples at a sample rate of $8f_{sc}$ and having twice the line frequency of the input interlaced video signal.

[0021] The chrominance signal provided by the circuit 102 is applied to a line doubler circuit 104. The circuit 104 doubles the chrominance samples for each line of the current field and separates the samples into separate (R-Y) and (B-Y) color difference signals. The line-doubled samples are provided at a sample rate of $8f_{sc}$, twice the line rate of the input interlaced video signal. The output signals Y, (R-Y) and (B-Y) provided by the line interpolator 106 and the line doubler 104 are applied to a matrix circuit 108 which combines the signals to produce primary color signals R, G and B which may be used to drive a display device (not shown).

[0022] Figure 1B is a block diagram of line interpolation circuitry suitable for use as the line interpolator 106, shown in Figure 1A. This circuit receives an interlace-scan luminance signal, such as that provided by the luminance/chrominance separation circuit 102, shown in Figure 1A, and applies the signal to a 262H delay line 110. The current received interlaced luminance signal is summed with the signal delayed by 262 horizontal line intervals in the summing circuit 114. The output signal of the 262H delay line is also applied to the input terminal of a 1H delay line 112 to provide a signal delayed by 263 horizontal line intervals. The output signal of the delay line 112 is applied to one input port of a summing circuit 116. The other input port of the summing circuit 116 is coupled to receive the current interlaced luminance signal. The output signal of the summing circuit 114 is the current line summed with the line from the previous field that is immediately below the current line in the displayed image. Similarly, The output signal of the summing circuit 116 is the sum of the currently received line of luminance data and the line of luminance data from the previous field that is immediately above the current line in the displayed image.

[0023] The output signals of the summing circuits of 114 and 116 are applied to respective time compression circuits 120 and 118. Each of the circuits 120 and 118 is essentially a first-in-first-out (FIFO) memory having a sufficient number of cells to hold one horizontal line interval of samples. In the exemplary embodiment of the invention, each of the FIFO memories holds at least 910 pixel data values. Data value are stored into the memories 120 and 118 as they are produced by the summing circuits 114 and 116 at the interlace-scan sample rate (e.g. $4f_{sc}$) and then are alternately read out of the memories 120 and 118 at twice the input sample rate (e.g. $8f_{sc}$). Thus, the output signal of the circuitry shown in Figure 1 has twice as many video lines as the input signal, each video line having the same number of samples as a line of the input signal. Thus, the output signal of the circuit shown in Figure 1 is a non-interlaced video signal each line of each frame of the non-interlaced video signal containing video information from two fields of the input interlaced video signal.

[0024] The clock signals that control the time compression circuits 118 and 120 are generated by the sync separator and clock generator 128 shown in Figure 1C. This circuit receives the interlaced video signal and generates from this signal a pixel clock signal, CLOCK, a frequency doubled signal, 2xCLK which has a frequency that is twice the frequency of the pixel clock signal and a signal, 2H, which has a frequency of twice the line frequency of the input interlaced video signal and which changes state each half line of the input video signal. The sync separator and clock generator 128 may include, for example, a sync separator circuit which separates the horizontal synchronization pulses and the color burst signal from the interlaced video signal and two phase locked loops, one which is synchronized to the horizontal sync pulses to generate the signal 2H and one which is synchronized to the color burst signal to produce the signals CLOCK and 2xCLK. In the exemplary embodiment of the invention, the signal CLOCK has a frequency of 4 times the color subcarrier frequency ($4f_{sc}$) of the input interlaced NTSC video signal and the signal 2xCLK has a frequency of $8f_{sc}$.

[0025] The signal CLOCK is applied to the write clock input of the 1H (FIFO) memories 120 and 118. Responsive to this signal, data provided by the summing circuits 114 and 116 is stored into the FIFO memories on a pixel by pixel basis as it is generated. The read clock signals

for the FIFO memory 120 are generated by an inverter 124 and AND gate 126. The inverter 124 inverts the signal 2H provided by the circuitry 128 and applies it to one input port of the AND gate 126. The other input terminal of the AND gate 126 is coupled to receive the signal 2xCLK. The AND gate 126 provides clock signals at twice the input pixel rate but for only one half line interval. Thus, one line of data from the summing circuit 114 is read out of the 1H FIFO memory 120 in one half horizontal line interval.

[0026] The read clock signal for the 1H FIFO 118 is generated by an AND gate 122 which is coupled to receive the signal 2xCLK and the 2H signal. The output signal of this AND gate provides clock pulses at the 2xCLK rate for every sample of input video data in the line but in the opposite half of the input horizontal line interval from the circuit 126.

[0027] In operation, input data is provided to the 1H FIFO 118 for one-half of one line interval. When the one-half line interval point is reached, data is read out of the FIFO 118 for one-half line interval but at twice the rate at which it was written into the FIFO. Thus, an entire video line of data is read out of the FIFO 18 in one-half line interval. For FIFO 120, an entire line of data is written into the FIFO and is then read out of the FIFO in one-half line interval. The first pulse of the write clock signal which writes a new line of data into the FIFO 120 is synchronized to occur immediately after the first clock pulse of the read clock signal which reads data out of the FIFO 120.

[0028] When data is provided by the FIFO 118, the multiplexer 130 is conditioned, by the signal 2H, to pass that data as the progressive-scan video signal. When data is provided by the FIFO 120, however, the multiplexer 130 is conditioned to provide that data as the progressive-scan video signal.

[0029] While the timing described above for the FIFO memories 118 and 120 is theoretically possible, actual FIFO memory devices may need more than 1H memory (e.g. 910 memory locations) in order to implement the time compression function described above.

[0030] As an alternative to the embodiment shown in Figure 1B, it is contemplated that the positions of the 262H delay line 110 and the 1H delay line 112 may be switched, the connections 115 and 113 broken (as indicated by the X's), and the connections 117 and 111 (shown in phantom) added in their place. In this alternative embodiment, the line from the delayed field is added to the lines immediately above and below it in the current field. Using the notation of Figure 2A, line 212B is simultaneously and separately interpolated with lines 210A and 210B in order to generate the two output lines of the progressive scan video signal.

[0031] Figure 2B is a vertical temporal diagram which shows several interlaced frames, numbered 1, 2, and 3. Each frame including a lower field "L" and upper field "U". The columns of circles in Figure 2B represent individual lines of the video fields. As shown in Figure 2B, the lines 210 of the lower field are positioned between the lines 212 of the upper field in the displayed image. The vertical temporal diagram shown in Figure 2B may be considered to be the image scan diagram shown in Figure 2A rotated out of the page such that the image lines go into the page.

[0032] Figure 2C illustrates the operation of the circuitry shown in Figure 1B. Each of the ellipses 214 and 216 shown in Figure 2C represents an interpolation operation performed by one of the summing circuits 116 and 114 shown in Figure 1B. For example, the ellipse 216 represents the summing of current interlaced video signal line 210A with delayed video signal line 212A by the summing circuit 116. Similarly, the ellipse 214 represents the summing of the current interlaced video signal line 210A and the delayed interlaced video signal line 212B.

[0033] Because the temporal position of the two input lines to the interpolation circuitry shown in Figure 1B are separated by a field time interval, the temporal position of the resulting interpolated line lies in the center of that field time interval. This is illustrated in Figure 2D. In Figure 2D, the interpolated frames are shown as columns of diamonds between the columns of circles that represent the fields of the input image. As shown in Figure 2D, interpolated line 220A is generated from original lines 210A and 212A. Interpolated line 220B is generated from input interlaced line 210A and 212B. Interpolated lines 220C and 220D are generated in the same way from interpolated input lines 210B and 212B and 210B, and 212C, respectively Figure 2E shows the interpolated lines of the output non-interlaced frames with the input interlaced lines removed.

[0034] Figure 3 is a graph showing the vertical resolution of the output non-interlaced video signal. The characteristic shown in Figure 3 represents a low pass vertical filtering of the input video image. Figure 4 is a graph of amplitude versus sample rate which illustrates the temporal resolution of the signal provided by the circuitry shown in Figure 1B. This Figure shows that there is a reduction in temporal resolution of the interlaced video signal by the interpolation process which produces the non-interlaced video signal.

[0035] The reduction in temporal resolution by the circuitry shown in Figure 1B, however, is comparable to the temporal resolution of a signal produced by a standard CCD television camera. Curve 512 in Figure 5 illustrates the temporal resolution of a field rate video CCD camera. The roll off shown in this characteristic is the result of integration of pixel data in the CCD camera over one field interval. Curve 510 of Figure 5 similarly shows the temporal response of a frame integrated video CCD camera. As shown, the temporal resolution of signals provided by a frame integrated camera is considerably less than that provided by field integrated video cameras. Finally, Figure 514 shows the temporal response characteristic of a shuttered CCD camera. Shuttered cameras integrate light quickly and for a shorter time in-

terval than either a frame interval or a field interval and thus, have a higher temporal resolution than either frame integrated or field integrated cameras.

[0036] From the graph shown in Figure 5, it is apparent that the circuitry shown in Figure 1B would have a negligible effect on the temporal resolution of a video signal produced by a frame integrated or field integrated camera however it may have a greater effect on a shuttered camera.

[0037] The circuitry shown in Figure 1B operates on a comb-filtered luminance signal generated by the luminance/chrominance separation filter 102 of Figure 1A. While this circuitry produces good results for most images, for some images there may be blurring along the horizontal lines of the image or even double images where there is movement between the two fields of a video signal. These artifacts are caused by the inclusion of high-frequency horizontal video information in the interpolated non-interlace-scan video signal and by horizontal motion in the image between the two fields that constitute the image frame. When this motion occurs, the pixels of the two fields that are being averaged to produce a pixel of non-interlaced frame may not represent the same video information. When the image includes a weak vertical edge, a blurring of the edge may result. When the image includes a strong vertical edge, it may contribute to pixels at different points on the line, resulting in an apparent double edge in the video image.

[0038] The circuitry shown in Figure 6 is designed to mitigate these blurring or double line artifacts. Essentially, this circuitry applies the line interpolation only to the low horizontal frequency components of the video image and augments these interpolated lines with high frequency video information taken from only one of the component fields. The circuitry shown in Figure 6 may receive either the interlaced luminance signal provided by the luminance/chrominance separation circuitry 102 shown in Figure 1A or it may receive an interlaced composite video signal, including both luminance and chrominance components.

[0039] In Figure 6, the interlaced input signal is applied to a low pass filter 610 and to one input port of a subtracting circuit 612. The other input port of the subtracting circuit 612 is coupled to receive the output signal of the low pass filter 610. The output signal of the low pass filter 610 is also applied to the line interpolation circuitry 106 which may be the same as that shown in Figure 1B. The output signal of the subtracting circuit 612, thus, represents only the high horizontal frequency components of the interlaced video signal.

[0040] If the input signal to the circuitry shown in Figure 6 is a composite video signal, the signal provided by the subtracting circuit 612 is applied to an optional luminance/chrominance separation circuit 102' (shown in phantom) which separates the chrominance signal components from the high frequency luminance signal components and provides the luminance signal components to a line repeater circuit 616. In this alternative embodiment of the invention, the separated chrominance signal is applied to the line doubling circuitry 104 shown in Figure 1A.

[0041] If, however, the input signal to the circuitry shown in Figure 6 is the comb-filtered luminance signal provided by the luminance/chrominance separation circuit 102 shown in Figure 1A, then the circuit 102' is not needed and the high-frequency luminance signal is applied to the line repeater circuit 616 directly from the subtracting circuit 612.

[0042] The exemplary line repeater circuit 616 operates in the same way as the line doubling circuit 104, described above, to produce non-interlaced lines of video samples in which the horizontal high frequency information from each line in the current input video field occurs twice, on adjacent lines, in the output video frame. The line repeater circuit 616 applies these high frequency components to all lines of the non-interlaced signal provided by the line interpolator 614, by summing the corresponding samples of non-interlaced signal and the high frequency video information in a summing circuit 618.

[0043] Figure 7 is a block diagram of a line repeat circuit suitable for use in the circuitry shown in Figure 6. In Figure 7, the input signal is applied to a 1H FIFO memory 710 which also receives signals provided by a clock and pulse generator 712. These signals include an input clock signal, f_s, at the input sample rate and an output clock signal, $2f_s$ at twice the input sample rate. The address counter for the input FIFO 710 is reset by a line rate pulse. And the output address counter for the FIFO 710 is reset by a pulse having double the frequency of the line rate pulse. In operation, when one-half of the input line has been written into the FIFO, the double line rate pulse resets the output counter and the stored line of data is read out at twice the rate at which it was written in. One-half line interval after the occurrence of the read reset pulse, the data stored in the FIFO 710 has been read out for the first time and the read clock is again reset to read the data out a second time, during the next one-half line interval. Shortly after the read clock is reset, the write clock is reset causing a new line of data to begin to be stored into the cells of the FIFO memory 710 that were just read responsive to the read clock signal. As set forth above with reference to the FIFO memories 118 and 120 shown in Figure 1, in a practical implementation, the FIFO memory 710 may need some additional cells beyond the 1H number of cells in order to operate properly.

[0044] The circuitry shown in Figure 7 simply doubles the lines from one field and applies them to the respective lines of the interpolated frame. This, however, may result in diagonal artifacts in the non-interlaced image. An alternative scheme to the line repeat scheme shown in Figure 7, is the line interpolation filter shown in Figure 8. This circuit receives the high frequency luminance information into a 1H delay line 810 and also applies the high frequency information to gain adjust circuits 612A

and 612C. The output signal of the 1H delay line is applied to gain adjust circuits 812B and 812D. The output signals provided by gain adjusted circuits 812A and 812D are applied to a summing circuit 814 which produces a signal that is, in turn, summed with the output signal provided by the summing circuit 114 shown in Figure 1B. The output signals of gain adjust circuits 812C and 812D are applied to a summing circuit 816 which produces an output signal that is added to the output signal provided by the summing circuit 116 shown in Figure 1B. By setting the gain adjust circuits 812A and 812B to, for example, .25 and .75 respectively and the gain circuits 812C and 812D to .75 and .25 respectively, vertical phase information that would otherwise be lost by the line repeat circuitry may be partially regained through interpolation.

[0045] While the invention has been described in terms of an NTSC video signal processing circuit, it is contemplated that it may be used to convert any interlace scan video signal to a non-interlace or progressive scan video signal. One skilled in the art of designing video signal processing circuits could readily construct such circuitry given the above description of the invention.

[0046] While the invention has been described in terms of exemplary embodiments, it is contemplated that it may be practiced as outlined above within the scope of the appended claims.

Claims

1. An interlace-scan to progressive-scan video signal conversion system comprising:

   a terminal for receiving an interlace-scan video signal;

   a low-pass filter (610) which attenuates relatively high frequency components of the interlace scan video signal relative to relatively low frequency components to provide a low-pass filtered interlace-scan video signal,

   a subtracter (612) which subtracts the low-pass filtered interlace-scan video signal from the received interlace-scan video signal to provide a high-pass filtered interlace scan video signal;

   an interpolation circuit (106) including:

   a first delay element (110), coupled to receive the low-pass filtered interlace-scan video signal for delaying the low-pass filtered interlace-scan video signal by a number, N, of horizontal line intervals to produce a first delayed video signal, wherein N horizontal line intervals is less than one field period but N+1 horizontal line intervals is greater than one field period;

   a second delay element (112), coupled to the first delay element (110) for delaying the first delayed video signal by one horizontal line interval to produce a second delayed video signal;

   a first interpolator (114) which combines the low-pass filtered interlace-scan video signal with the first delayed video signal to produce a first interpolated signal;

   a second interpolator (116) which combines the low-pass filtered interlace-scan video signal with the second delayed video signal to produce a second interpolated signal;

   a first speed-up memory (120) coupled to the first interpolator (114) to receive samples of the first interpolated signal at a first sample rate and to provide the samples of the first interpolated signal, as an output signal, at a second sample rate which is twice the first sample rate;

   a second speed-up memory (118) coupled to the second interpolator (116) to receive samples of the second interpolated signal at the first sample rate and to provide the samples of the second interpolated signal, as an output signal, at the second sample rate;

   a multiplexer (130), coupled to the first and second speed-up memories (120, 118), to alternately provide the output signals of the first and second speed-up memories (120, 118) as a low-pass filtered progressive-scan video signal; and

   the system further includes

   a line doubling circuit (616) coupled to receive the high-pass filtered interlace scan video signal for generating a progressive-scan high-pass filtered video signal by repeating each line of the high-pass filtered interlace scan video signal; and

   means (618) for adding the progressive-scan high-pass filtered video signal to the signal provided by the multiplexer (130) to produce the progressive scan video signal.

2. An interlace-scan to progressive-scan video signal conversion system according to claim 1, further comprising:

   a third delay element (810) which delays the high-pass filtered interlace scan video signal by one horizontal line interval of the interlace-scan video signal to produce a delayed high-pass filtered video signal;

   a third interpolator (814) which combines the

high-pass filtered interlace scan video signal and the delayed high-pass filtered video signal in a first proportion to produce a first interpolated high-pass filtered video signal;

a fourth interpolator (816) which combines the high-pass filtered interlace scan video signal and the delayed high-pass filtered video signal in a second proportion, different from the first proportion, to produce a second interpolated high-pass filtered video signal;

means for adding the first interpolated high-pass filtered video signal to the first interpolated signal; and

means for adding the second interpolated high-pass filtered video signal to the second interpolated signal.

3. An interlace scan to progressive scan video signal conversion system according to claim 2, wherein the received interlace scan video signal is a composite video signal including luminance signal components and chrominance signal components and the system further comprises luminance/chrominance separation circuitry, coupled to receive the high-pass filtered interlace scan video signal, which separates the chrominance signal components from the high-pass filtered interlace-scan video signal before providing the high-pass filtered interlace-scan video signal to the third delay element (810) and to the third and fourth interpolators (814, 816).

4. An interlace-scan to progressive-scan video signal conversion system according to one of claims 1 to 3, wherein the received interlace-scan video signal is a luminance component signal.

5. An interlace-scan to progressive-scan video signal conversion system according to one of the preceding claims, wherein

the interlace-scan video signal is an interlace-scan luminance video signal; and

N equals 262.

6. A method for converting an interlace-scan video signal having a first sample rate to a progressive-scan video signal having a second sample rate greater than the first sample rate, the method comprising the steps of:

a) low-pass filtering the interlace scan video signal to provide a low-pass filtered interlace-scan video signal;

b) subtracting the low-pass filtered interlace-scan video signal from the interlace-scan video signal to provide a high-pass filtered interlace scan video signal;

c) converting each line of samples of the high-pass filtered interlace-scan video signal into two lines of samples at the second sampling rate to produce a progressive scan high-pass filtered video signal;

d) providing a first delayed video signal representing the low-pass filtered interlace-scan video signal, the first delayed video signal and the low-pass filtered interlace-scan video signal having a difference in time of N horizontal line intervals, N being an integer such that N horizontal line intervals is less than one field period but N+1 horizontal line intervals is greater than one field period;

e) providing a second delayed video signal representing the low-pass filtered interlace-scan video signal, the second delayed video signal and the low-pass filtered interlace-scan video signal having a difference in time of N+1 horizontal line intervals;

f) interpolating between the low-pass filtered video signal and the first delayed video signal to produce a first interpolated signal;

g) interpolating between the low-pass filtered video signal and second delayed video signal to produce a second interpolated signal;

h) doubling the sample rate of the first and second interpolated signals to produce double-speed first and second interpolated signals;

i) alternately providing one horizontal line of samples of the double-speed first and second interpolated signals, respectively, and adding the progressive-scan high-pass filtered video signal to the signal to produce the progressive-scan video signal.

7. A method according to claim 6, further comprising the steps of:

delaying the high-pass filtered interlace scan video signal by one horizontal line interval of the interlace-scan video signal to produce a delayed high-pass filtered video signal;

interpolating between the high-pass filtered interlace scan video signal and the delayed high-pass filtered video signal in a first proportion to produce a first interpolated high-pass filtered video signal;

interpolating between the high-pass filtered interlace scan video signal and the delayed high-pass filtered video signal in a second proportion, different from the first proportion, to produce a second interpolated high-pass filtered video signal;

adding the first interpolated high-pass filtered video signal to the first interpolated signal; and

adding the second interpolated high-pass filtered video signal to the second interpolated signal.

8. A method according to claim 7, wherein the received interlace scan video signal is a composite video signal including luminance signal components and chrominance signal components and the method further comprises the step of separating the chrominance signal components from the high-pass filtered interlace-scan video signal before delaying the high-pass filtered interlace-scan video signal and before interpolating between the high-pass filtered interlace-scan video signal and the delayed high-pass filtered video signal.

Patentansprüche

1. System zur Umwandlung eines mit Zeilensprung abgetasteten in ein fortlaufend abgetastetes Video-Signal mit:

einem Anschluss zum Empfangen eines Zeilensprung-Abtastungs(interlace-scan) Video-Signals;
einem Tiefpassfilter (610), welcher relativ hochfrequente Komponenten des Zeilensprung-Abtastungs-Video-Signals dämpft relativ zu relativ niederfrequenten Komponenten, um ein Tiefpass-gefiltertes Zeilensprung-Abtastungs-Video-Signal zur Verfügung zu stellen,
einem Subtrahierer (612), welcher das Tiefpass-gefilterte Zeilensprung-Abtastungs Video-Signal von dem empfangenen Zeilensprung-Abtastungs-Video-Signal subtrahiert, um ein Hochpass-gefiltertes Zeilensprung-Abtastungs-Video-Signal zur Verfügung zu stellen;
einer Interpolations-Schaltung (106), welche aufweist:

ein erstes Verzögungselement (110), verschaltet um das Tiefpass-gefilterte Zeilensprung-Abtastungs-Video-Signal zu empfangen zur Verzögerung des Tiefpass-gefilterten Zeilensprung-Abtastungs-Video-Signals um eine Anzahl N von horizontalen Zeilen-Intervallen, um ein erstes verzögertes Video-Signal zu erzeugen, wobei N horizontale Zeilen-Intervalle weniger sind als eine Halbbild(field)-Periode, jedoch N+1 1 horizontale Zeilen-Intervalle sind mehr als eine Halbbild-Periode;
ein zweites Verzögerungselement (112), verschaltet mit dem ersten Verzögerungselement (110), zum Verzögern des ersten verzögerten Video-Signals um ein horizontales Zeilen-Intervall, um ein zweites verzögertes Video-Signal zu erzeugen;
einen ersten Interpolator (114), welcher das Tiefpass-gefilterte Zeilensprung-Abtastungs-Video-Signal kombiniert mit dem ersten verzögerten Video-Signal, um ein erstes interpoliertes Signal zu erzeugen;
einen zweiten Interpolator (116), welcher das Tiefpass-gefilterte Zeilensprung-Abtastungs-Video-Signal kombiniert mit dem zweiten verzögerten Video-Signal, um ein zweites interpoliertes Signal zu erzeugen;
einen ersten Beschleunigungs(speed-up) -Speicher (120), welcher mit dem ersten Interpolator (114) verschaltet ist, um Abtastwerte des ersten interpolierten Signals bei einer ersten Abtast-Rate zu empfangen und um die Abtastwerte des ersten interpolierten Signals zur Verfügung zu stellen, als ein Ausgabe-Signal, bei einer zweiten Abtast-Rate, welche das Zweifache der ersten Abtast-Rate ist;
einen zweiten Beschleunigungs-Speicher (118), welcher mit dem zweiten Interpolator (116) verschaltet ist, um Abtastwerte des zweiten interpolierten Signals bei der ersten Abtast-Rate zu empfangen und um die Abtastwerte des zweiten interpolierten Signals zur Verfügung zu stellen, als ein Ausgabe-Signal, bei der zweiten Abtast-Rate;
einen Multiplexer (130), welcher mit den ersten und zweiten Beschleunigungs-Speichern (120, 118) verschaltet ist, um alternierend bzw. abwechselnd die AusgabeSignale der ersten und zweiten Beschleunigungs-Speicher (120, 118) zur Verfügung zu stellen, als ein Tiefpass-gefiltertes fortlaufend abgetastetes (prgressive-scan) Video-Signal; und
das System umfasst weiter

eine Zeilen-Verdopplungs-Schaltung (616), welche verschaltet ist, um das Hochpass-gefilterte Zeilensprung-Abtastungs-Video-Signal zu empfangen zum Erzeugen eines fortlaufend abgetasteten Hochpass-gefilterten Video-Signals durch Wiederholen jeder Zeile des Hochpass-gefilterten Zeilensprung-Abtastungs-Video-Signals; und
eine Vorrichtung (618) zum Addieren des fortlaufend-abgetasteten Hochpass-gefilterten Video-Signals zu dem Signal, welches von dem Multiplexer (130) zur Verfügung gestellt wird, um das fortlaufend abgetastete Video-Signal zu erzeugen.

2. System zum Umwandeln eines mit Zeilensprung abgetasteten in ein fortlaufend abgetastetes Video-Signal nach Anspruch 1 weiter aufweisend:

ein drittes Verzögerungselement (810), wel-

ches das Hochpass-gefilterte Zeilensprung-abgetastete Video-Signal um ein horizontales Zeilen-Intervall des Zeilensprung-abgetasteten Video-Signals verzögert, um ein verzögertes Hochpass-gefiltertes Video-Signal zu erzeugen;
einen dritten Interpolator (814), welcher das Hochpass-gefilterte Zeilensprung-abgetastete Video-Signal und das verzögerte Hochpass-gefilterte Video-Signal mit einem ersten Verhältnis kombiniert, um ein erstes interpoliertes Hochpass-gefiltertes Video-Signal zu erzeugen;
einen vierten Interpolator (816), welcher das Hochpass-gefilterte Zeilensprung-abgetastete Video-Signal und das verzögerte Hochpass-gefilterte Video-Signal mit einem zweiten Verhältnis kombiniert, welches von dem ersten Verhältnis verschieden ist, um ein zweites interpoliertes Hochpass-gefiltertes Video-Signal zu erzeugen;
eine Vorrichtung zum Addieren des ersten interpolierten Hochpass-gefilterten Video-Signals zu dem ersten interpolierten Signal; und
eine Vorrichtung zum Addieren des zweiten interpolierten Hochpass-gefilterten Video-Signals zu dem zweiten interpolierten Signal.

3. System zum Umwandeln eines mit Zeilensprung abgetasteten in ein fortlaufend abgetastetes Video-Signal nach Anspruch 2, wobei das empfangene Zeilensprung-abgetastete Video-Signal ein zusammengesetztes Video-Signal ist, welches Leuchtdichte- bzw. Luminanz-Signal-Komponenten und Chrominanz-Signal-Komponenten enthält, und das System weist weiter eine Luminanz/Chrominanz-Trenn-Schaltung auf, welche so verschaltet ist, um das Hochpass-gefilterte Zeilensprung-abgetastete Video-Signal zu empfangen, welche die Chrominanz-Signal-Komponenten von dem Hochpass-gefilterten Zeilensprung-abgetasteten Video-Signal trennt, bevor das Hochpass-gefilterte Zeilensprung-abgetastete Video-Signal dem dritten Verzögerungselement (810) und den dritten und vierten Interpolatoren (814, 816) zur Verfügung gestellt wird.

4. System zum Umwandeln eines mit Zeilensprung abgetasteten in ein fortlaufend abgetastetes Video-Signal nach einem der Ansprüche 1 bis 3, wobei das empfangene Zeilensprung-abgetastete Video-Signal ein Luminanz-Komponenten-Signal ist.

5. System zum Umwandeln eines mit Zeilensprung abgetasteten in ein fortlaufend abgetastetes Video-Signal nach einem der vorhergehenden Ansprüche, wobei
das Zeilensprung-abgetastete Video-Signal ein Zeilensprung-abgetastetes Luminanz-Video-Signal ist; und
N ist gleich 262.

6. Verfahren zum Umwandeln eines Zeilensprung-abgetasteten Video-Signals mit einer ersten Abtast-Rate in ein fortlaufend abgetastetes Video-Signal mit einer zweiten Abtast-Rate, welche größer ist als die erste Abtast-Rate, wobei das Verfahren die Schritte aufweist:

a) Tiefpass-Filtern des Zeilensprung-Abtastungs-Video-Signals, um ein Tiefpass-gefiltertes Zeilensprung-Abtastungs-Video-Signal zur Verfügung zu stellen;
b) Subtrahieren des Tiefpass-gefilterten Zeilensprung-Abtastungs-Video-Signals von dem Zeilensprung-Abtastungs-Video-Signal, um ein Hochpass-gefiltertes Zeilensprung-Abtastungs-Video-Signal zur Verfügung zu stellen;
c) Umwandeln einer jeden Zeile der Abtastwerte des Hochpass-gefilterten Zeilensprung-abgetasteten Video-Signals in zwei Zeilen von Abtastwerten bei der zweiten Abtast-Rate, um ein fortlaufend abgetastetes Hochpass-gefiltertes Video-Signal zu erzeugen;
d) zur Verfügung stellen eines ersten verzögerten Video-Signals, welches das Tiefpass-gefilterte Zeilensprung-abgetastete Video-Signal zur Verfügung stellt, wobei das erste verzögerte Video-Signal und das Tiefpass-gefilterte Zeilensprung-abgetastete Video-Signal eine zeitliche Differenz von N horizontalen Zeilen-Intervallen haben, wobei N eine ganze Zahl ist, so dass N horizontale Zeilen-Intervalle weniger als eine Halbbild(field)-Periode sind, jedoch N+1 horizontale Zeilen-Intervalle sind größer als eine Halbbild-Periode;
e) zur Verfügung stellen eines zweiten verzögerten Video-Signals, welches das Tiefpass-gefilterte Zeilensprung-abgetastete Video-Signal darstellt, wobei das zweite verzögerte Video-Signal und das Tiefpass-gefilterte Zeilensprung-abgetastete Video-Signal eine zeitliche Differenz von N+1 horizontale Zeilen-Intervallen haben;
f) Interpolieren zwischen dem Tiefpass-gefilterten Video-Signal und dem ersten verzögerten Video-Signal, um ein erstes interpoliertes Signal zu erzeugen;
g) Interpolieren zwischen dem Tiefpass-gefilterten Video-Signal und dem zweiten verzögerten Video-Signal, um ein zweites interpoliertes Signal zu erzeugen;
h) Verdoppeln der Abtast-Rate der ersten und zweiten interpolierten Signale, um erste und zweite interpolierte Signale mit doppelter Geschwindigkeit (double-speed) zu erzeugen;

i) abwechselndes bzw. alternierendes zur Verfügung stellen einer horizontalen Zeile von Abtastwerten der ersten und zweiten interpolierten Signale mit verdoppelter Geschwindigkeit, und Addieren des fortlaufend-abgetasteten Hochpass-gefilterten Video-Signals zu dem Signal, um das fortlaufend abgetastete Video-Signal zu erzeugen.

7. Verfahren nach Anspruch 6, weiter aufweisend die Schritte:

Verzögern des Hochpass-gefilterten Zeilensprung-abgetasteten Video-Signals um ein horizontales Zeilenintervall des Zeilensprung-Abtastungs-Video-Signals, um ein verzögertes Hochpass-gefiltertes Video-Signal zu erzeugen;
Interpolieren zwischen dem Hochpass-gefilterten Zeilensprung-Abtastungs-Video-Signal und dem verzögerten Hochpass-gefilterten Video-Signal in einem ersten Verhältnis, um ein erstes interpoliertes Hochpass-gefiltertes Video-Signal zu erzeugen;
Interpolieren zwischen dem Hochpass-gefilterten Zeilensprung-Abtastungs-Video-Signal und dem verzögerten Hochpass-gefilterten Video-Signal in einem zweiten Verhältnis, welches von dem ersten Verhältnis verschieden ist, um ein zweites interpoliertes Hochpass-gefiltertes Video-Signal zu erzeugen;
Addieren des ersten interpolierten Hochpass-gefilterten Video-Signals zu dem ersten interpolierten Signal; und
Addieren des zweiten interpolierten Hochpass-gefilterten Video-Signals zu dem zweiten interpolierten Signal.

8. Verfahren nach Anspruch 7, wobei das empfangene Zeilensprung-Abtastungs-Video-Signal ein zusammengesetztes Video-Signal ist, welches Leuchtdichte- bzw. Luminanz-Signal-Komponenten und Chrominanz-Signal-Komponenten enthält, und das Verfahren weist weiter den Schritt auf des Trennens der Chrominanz-Signal-Komponenten von dem Hochpass-gefilterten Zeilensprung-Abtastungs-Video-Signal, vor dem Verzögern des Hochpass-gefilterten Zeilensprung-Abtastungs-Video-Signals und vor dem Interpolieren zwischen dem Hochpass-gefilterten Zeilensprung-Abtastungs-Video-Signal und dem verzögerten Hochpass-gefilterten Video-Signal.

Revendications

1. Système de conversion d'un signal vidéo à balayage entrelacé en un signal vidéo à balayage progressif, comportant :

un terminal pour recevoir un signal vidéo à balayage entrelacé,
un filtre passe-bas (610) qui atténue les composantes fréquentielles relativement hautes du signal vidéo à balayage entrelacé par rapport à des composantes fréquentielles relativement basses pour fournir un signal vidéo à balayage entrelacé ayant subi un filtrage passe-bas,
un soustracteur (612) qui soustrait le signal vidéo à balayage entrelacé ayant subi un filtrage passe-bas à partir du signal vidéo à balayage entrelacé reçu pour fournir un signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut,
un circuit d'interpolation (106) incluant :

un premier élément à retard (110), couplé pour recevoir le signal vidéo à balayage entrelacé ayant subi un filtrage passe-bas pour retarder le signal vidéo à balayage entrelacé ayant subi un filtrage passe-bas d'un nombre, N, d'intervalles de lignes horizontales pour produire un premier signal vidéo retardé, dans lequel N intervalles de lignes horizontales est inférieur à une période de trame mais N+1 intervalles de lignes horizontales est supérieur à une période de trame,
un deuxième élément à retard (112), couplé au premier élément à retard (110) pour retarder le premier signal vidéo retardé d'un intervalle de lignes horizontales pour produire un second signal vidéo retardé,
un premier interpolateur (114) qui combine le signal vidéo à balayage entrelacé ayant subi un filtrage passe-bas avec le premier signal vidéo retardé pour produire un premier signal interpolé,
un deuxième interpolateur (116) qui combine le signal vidéo à balayage entrelacé ayant subi un filtrage passe-bas avec le second signal vidéo retardé pour produire un second signal interpolé,
une première mémoire d'accélération (120) couplée au premier interpolateur (114) pour recevoir des échantillons du premier signal interpolé à une première fréquence d'échantillonnage et pour fournir les échantillons du premier signal interpolé, en tant que signal de sortie, à une seconde fréquence d'échantillonnage qui est égale au double de la première fréquence d'échantillonnage,
une seconde mémoire d'accélération (118) couplée au deuxième interpolateur (116) pour recevoir des échantillons du second

signal interpolé à la première fréquence d'échantillonnage et pour fournir les échantillons du second signal interpolé, en tant que signal de sortie, à la seconde fréquence d'échantillonnage,
un multiplexeur (130), couplé aux première et seconde mémoires d'accélération (120, 118), pour fournir d'une manière alternée les signaux de sortie des première et seconde mémoires d'accélération (120, 118) sous la forme d'un signal vidéo à balayage progressif ayant subi un filtrage passe-bas, et
le système inclut en outre
un circuit de doublage de ligne (616) couplé pour recevoir le signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut pour générer un signal vidéo ayant subi un filtrage passe-haut à balayage progressif en répétant chaque ligne du signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut,
des moyens (618) pour ajouter le signal vidéo ayant subi un filtrage passe-haut à balayage progressif au signal fourni par le multiplexeur (130) afin de produire le signal vidéo à balayage progressif.

2. Système de conversion d'un signal vidéo à balayage entrelacé en un signal vidéo à balayage progressif selon la revendication 1, comportant en outre :

un troisième élément à retard (810) qui retarde le signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut d'un intervalle de lignes horizontales du signal vidéo à balayage entrelacé afin de produire un signal vidéo ayant subi un filtrage passe-haut retardé,
un troisième interpolateur (814) qui combine le signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut et le signal vidéo ayant subi un filtrage passe-haut retardé dans une première proportion pour produire un premier signal vidéo ayant subi un filtrage passe-haut interpolé,
un quatrième interpolateur (816) qui combine le signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut et le signal vidéo ayant subi un filtrage passe-haut retardé dans une seconde proportion, différente de la première proportion, afin de produire un second signal vidéo ayant subi un filtrage passe-haut interpolé,
des moyens pour ajouter le premier signal vidéo ayant subi un filtrage passe-haut interpolé au premier signal interpolé, et
des moyens pour ajouter le second signal vidéo ayant subi un filtrage passe-haut interpolé au second signal interpolé.

3. Système de conversion d'un signal vidéo à balayage entrelacé en un signal vidéo à balayage progressif selon la revendication 2, dans lequel le signal vidéo à balayage entrelacé reçu est un signal vidéo composite incluant des composantes de signal de luminance et des composantes de signal de chrominance et le système comporte en outre un circuit de séparation luminance/chrominance, couplé pour recevoir le signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut, qui sépare les composantes de signal de chrominance du signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut avant de fournir le signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut au troisième élément à retard (810) et aux troisième et quatrième interpolateurs (814, 816).

4. Système de conversion d'un signal vidéo à balayage entrelacé en un signal vidéo à balayage progressif selon l'une quelconque des revendications 1 à 3, dans lequel le signal vidéo à balayage entrelacé reçu est un signal de composante de luminance.

5. Système de conversion d'un signal vidéo à balayage entrelacé en un signal vidéo à balayage progressif selon l'une quelconque des revendications précédentes, dans lequel
le signal vidéo à balayage entrelacé est un signal vidéo de luminance à balayage entrelacé, et
N est égal à 262.

6. Procédé pour convertir un signal vidéo à balayage entrelacé ayant une première fréquence d'échantillonnage en un signal vidéo à balayage progressif ayant une seconde fréquence d'échantillonnage supérieure à la première fréquence d'échantillonnage, le procédé comportant les étapes consistant à :

a) soumettre le signal vidéo à balayage entrelacé à un filtrage passe-bas pour fournir un signal vidéo à balayage entrelacé ayant subi un filtrage passe-bas,
b) soustraire le signal vidéo à balayage entrelacé ayant subi un filtrage passe-bas à partir du signal vidéo à balayage entrelacé pour fournir un signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut,
c) convertir chaque ligne d'échantillons du signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut en deux lignes d'échantillons à la seconde fréquence d'échantillonnage afin de produire un signal vidéo ayant subi un filtrage passe-haut à balayage progressif,
d) fournir un premier signal vidéo retardé représentant le signal vidéo à balayage entrelacé ayant subi un filtrage passe-bas, le premier si-

gnal vidéo retardé et le signal vidéo à balayage entrelacé ayant subi un filtrage passe-bas ayant une différence de temps égale à N intervalles de lignes horizontales, N étant un nombre entier tel que N intervalles de lignes horizontales est inférieur à une période de trame mais N+1 intervalles de lignes horizontales est supérieur à une période de trame,

e) fournir un second signal vidéo retardé représentant le signal vidéo à balayage entrelacé ayant subi un filtrage passe-bas, le second signal vidéo retardé et le signal vidéo à balayage entrelacé ayant subi un filtrage passe-bas ayant une différence de temps égale à N+1 intervalles de lignes horizontales,

f) effectuer une interpolation entre le signal vidéo ayant subi un filtrage passe-bas et le premier signal vidéo retardé pour produire un premier signal interpolé,

g) effectuer une interpolation entre le signal vidéo ayant subi un filtrage passe-bas et le second signal vidéo retardé pour produire un second signal interpolé,

h) doubler la fréquence d'échantillonnage des premier et second signaux interpolés pour produire des premier et second signaux interpolés à vitesse double,

i) fournir d'une manière alternée une ligne horizontale d'échantillons des premier et second signaux interpolés à vitesse double, respectivement, et ajouter le signal vidéo ayant subi un filtrage passe-haut à balayage progressif au signal afin de produire le signal vidéo à balayage progressif.

7. Procédé selon la revendication 6, comportant en outre les étapes consistant à :

retarder le signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut d'un intervalle de lignes horizontales du signal vidéo à balayage entrelacé pour produire un signal vidéo ayant subi un filtrage passe-haut retardé,

effectuer une interpolation entre le signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut et le signal vidéo ayant subi un filtrage passe-haut retardé dans une première proportion pour produire un premier signal vidéo ayant subi un filtrage passe-haut interpolé,

effectuer une interpolation entre le signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut et le signal vidéo ayant subi un filtrage passe-haut retardé dans une seconde proportion, différente de la première proportion, pour produire un second signal vidéo ayant subi un filtrage passe-haut interpolé,

ajouter le premier signal vidéo ayant subi un filtrage passe-haut interpolé au premier signal interpolé, et

ajouter le second signal vidéo ayant subi un filtrage passe-haut interpolé au second signal interpolé.

8. Procédé selon la revendication 7, dans lequel le signal vidéo à balayage entrelacé reçu est un signal vidéo composite incluant des composantes de signal de luminance et des composantes de signal de chrominance et le procédé comporte en outre l'étape consistant à séparer les composantes de signal de chrominance du signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut avant de retarder le signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut et avant d'effectuer une interpolation entre le signal vidéo à balayage entrelacé ayant subi un filtrage passe-haut et le signal vidéo ayant subi un filtrage passe-haut retardé.

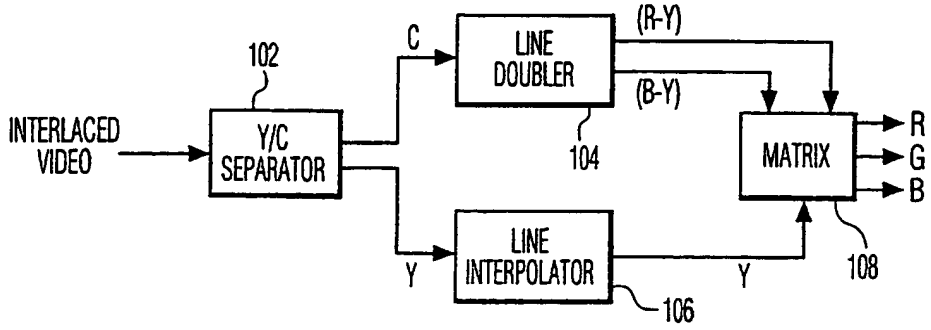


FIG. 1A

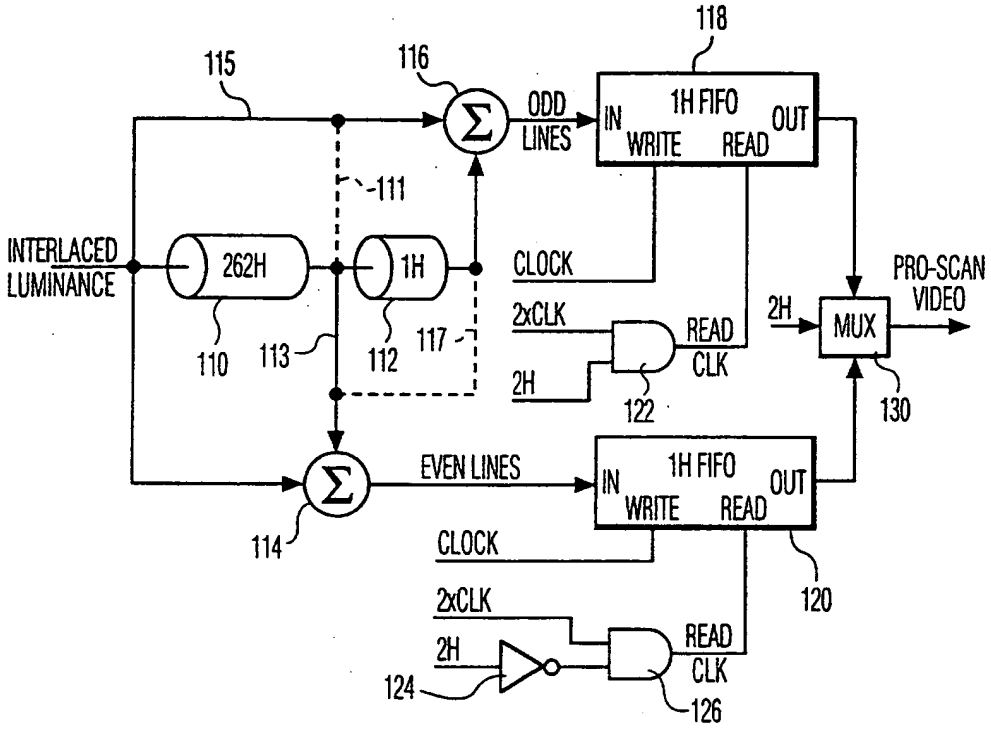


FIG. 1B

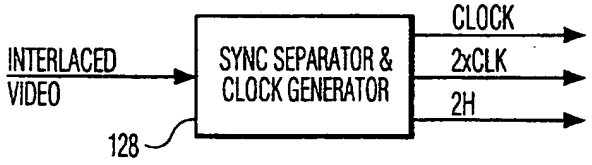
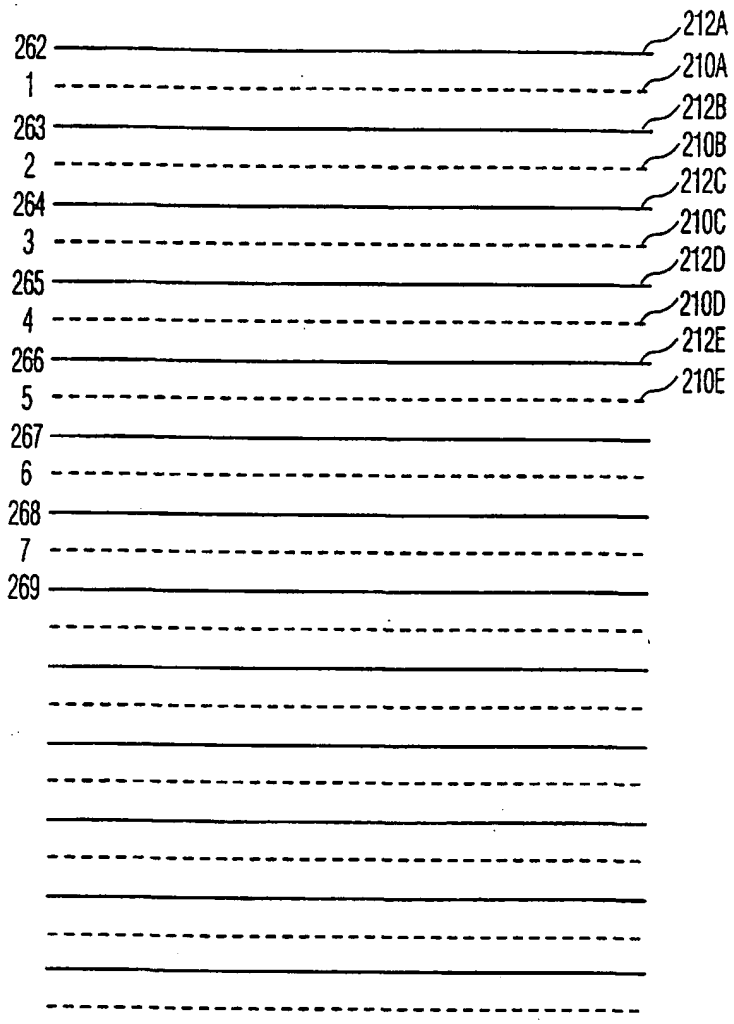


FIG. 1C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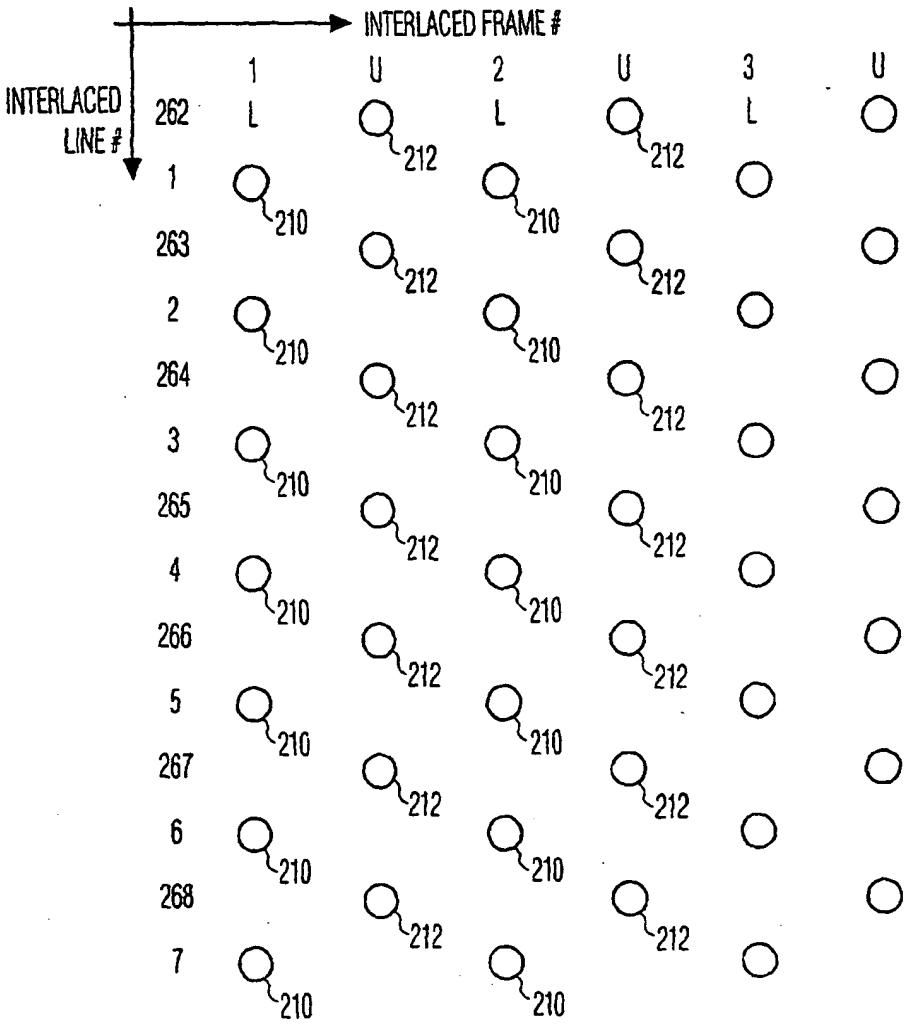
210C
212D
210D
212E
210E

FIG. 2A


INTERLACED FRAME #
INTERLACED LINE #
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U
2
U
3
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262
L
L
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263
2
264
3
265
4
266
5
267
6
268
7
210
212

FIG. 2B

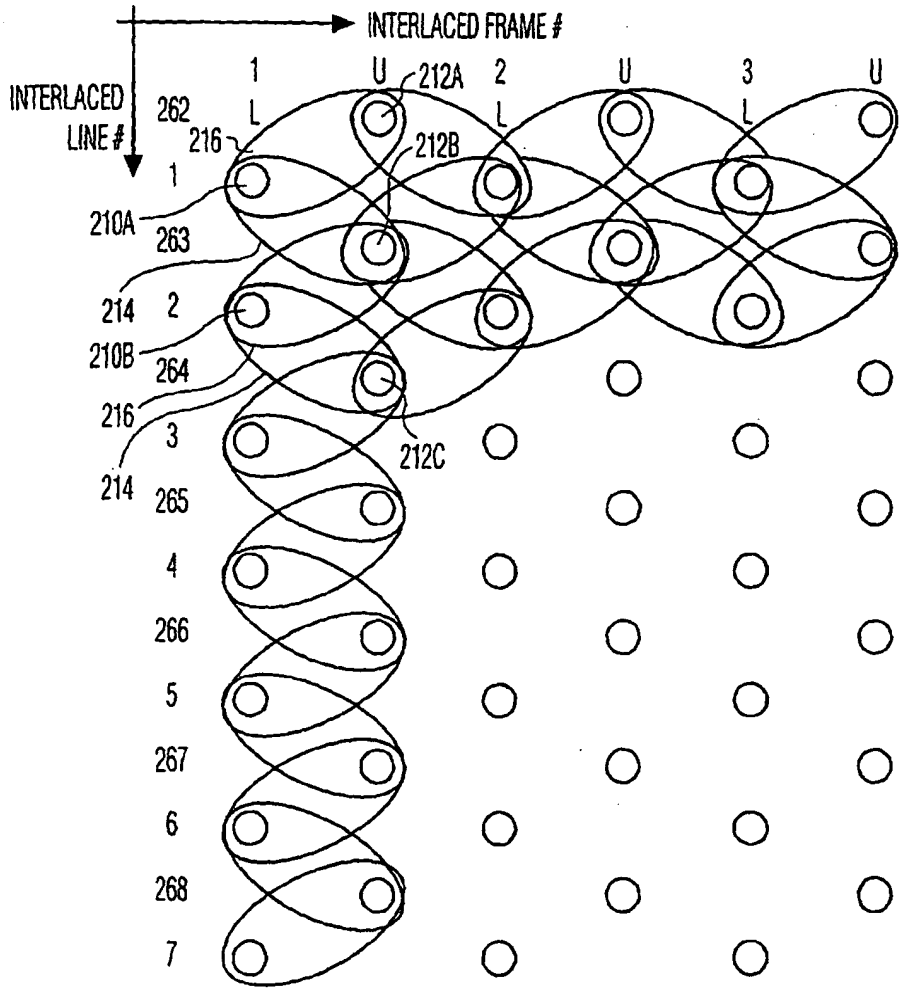
INTERLACED FRAME #
INTERLACED LINE #
1
U
212A
2
U
3
U
L
L
L
262
216
212B
1
210A
263
214
2
210B
264
216
3
212C
214
265
4
266
5
267
6
268
7

FIG. 2C

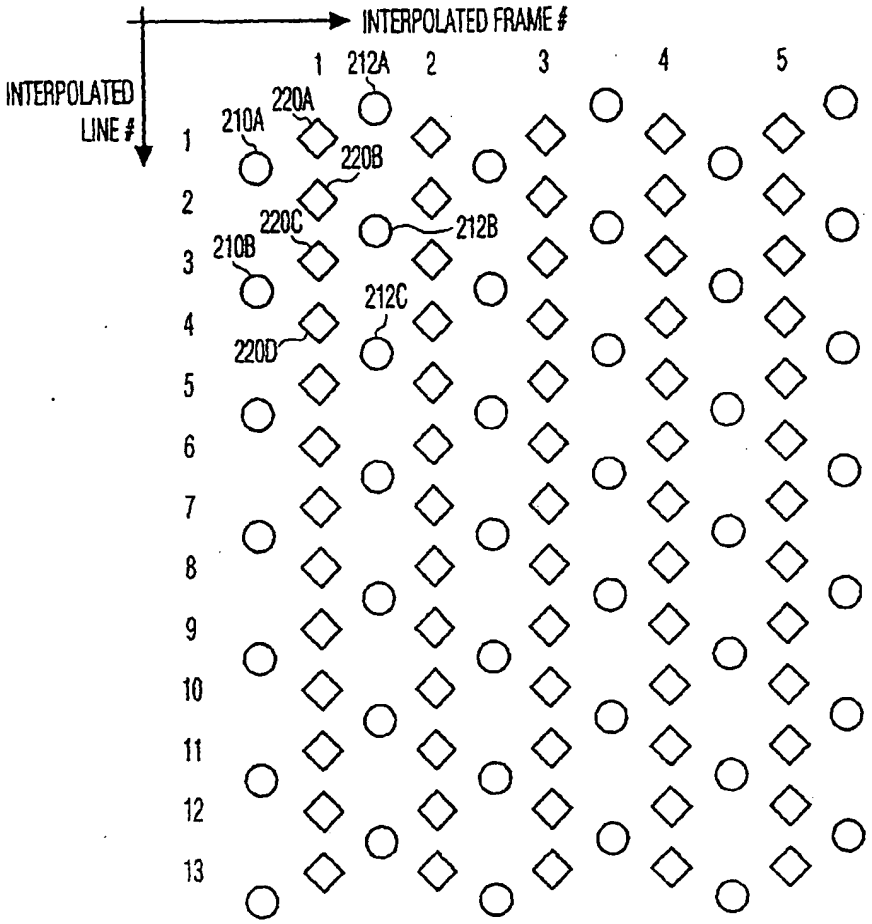
INTERPOLATED FRAME #
INTERPOLATED LINE #
1
212A
2
3
4
5
210A
220A
220B
220C
212B
210B
212C
220D
1
2
3
4
5
6
7
8
9
10
11
12
13

FIG. 2D

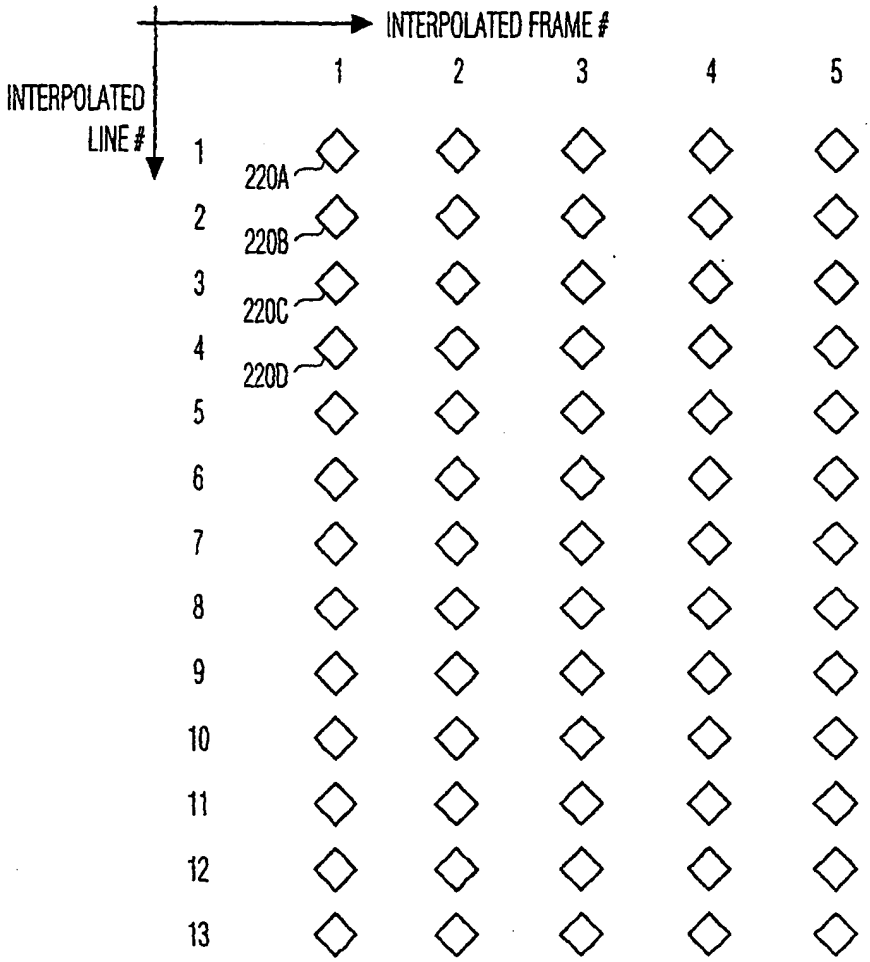
INTERPOLATED FRAME #
1
2
3
4
5
INTERPOLATED LINE #
1
2
3
4
5
6
7
8
9
10
11
12
13
220A
220B
220C
220D

FIG. 2E

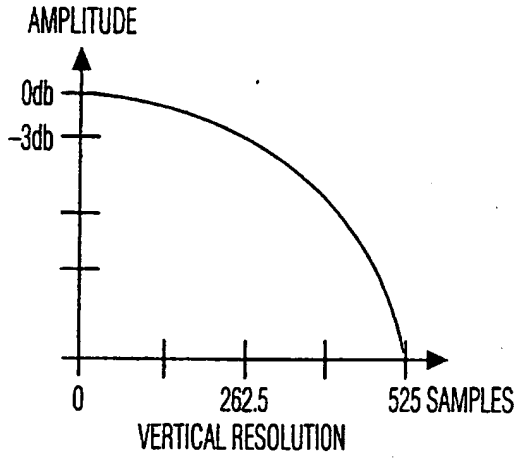

FIG. 3

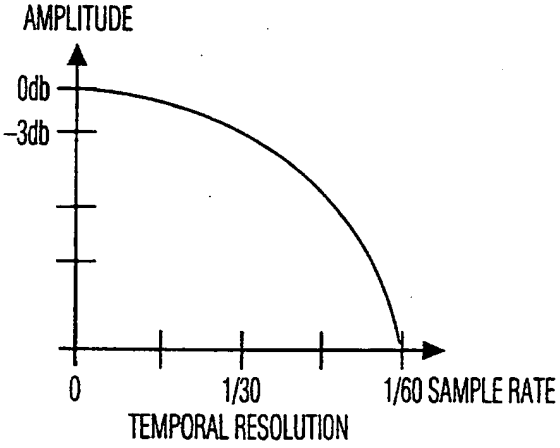

FIG. 4

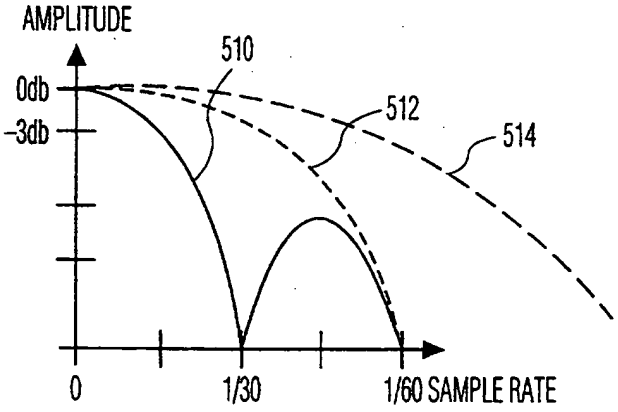

FIG. 5

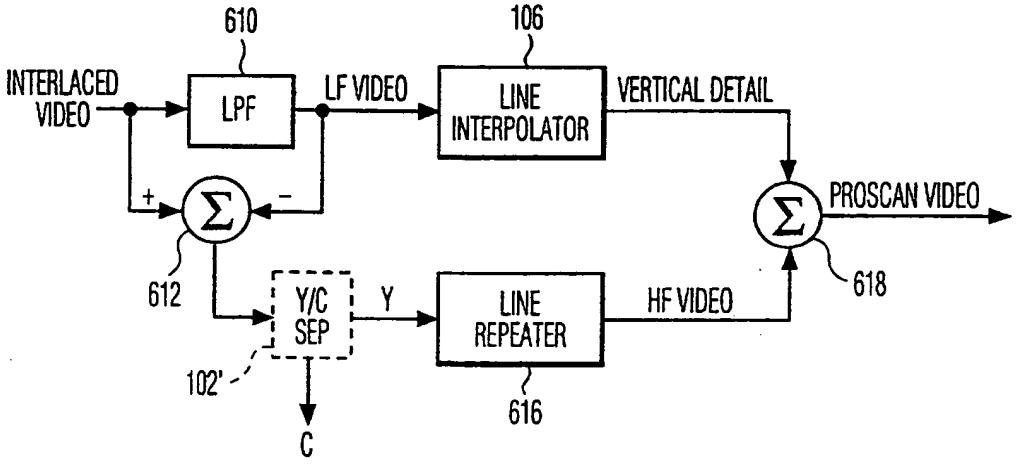
610
106
INTERLACED VIDEO
LPF
LF VIDEO
LINE INTERPOLATOR
VERTICAL DETAIL
+
−
PROSCAN VIDEO
612
618
Y/C SEP
Y
LINE REPEATER
HF VIDEO
102'
616
C

FIG. 6

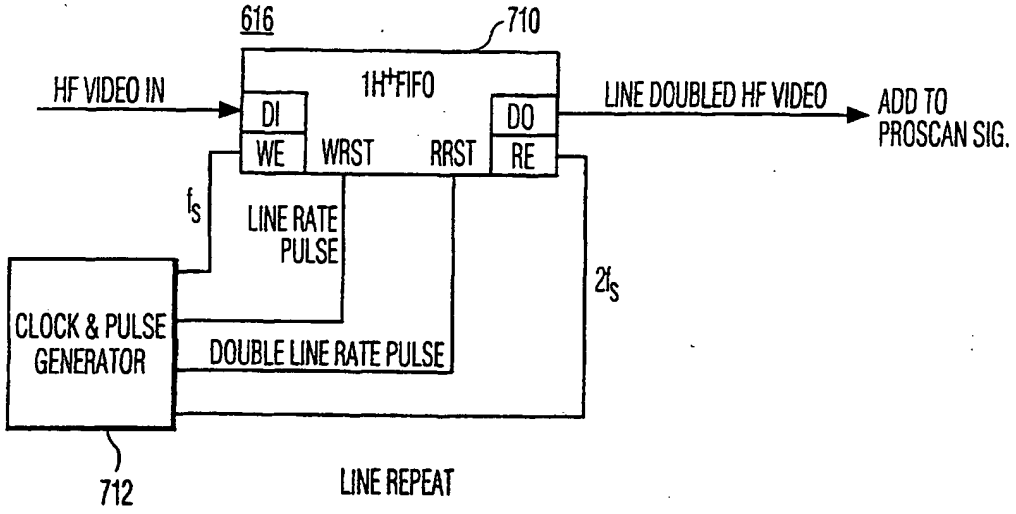
616
710
1H+FIFO
HF VIDEO IN
DI
WE
WRST
RRST
DO
RE
LINE DOUBLED HF VIDEO
ADD TO PROSCAN SIG.
f_S
LINE RATE PULSE
$2f_S$
CLOCK & PULSE GENERATOR
DOUBLE LINE RATE PULSE
712
LINE REPEAT

FIG. 7

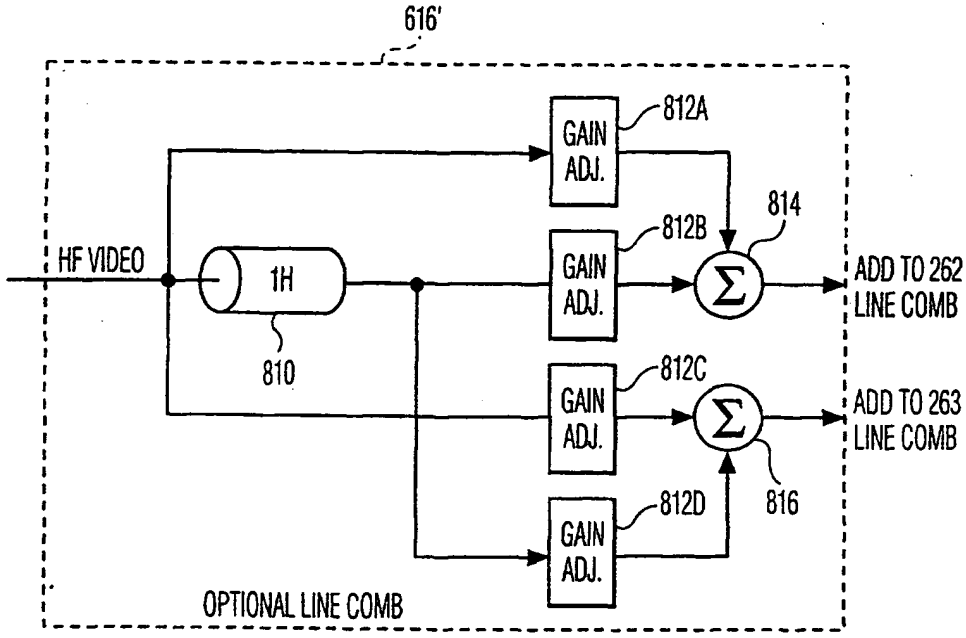
616'
812A
GAIN ADJ.
814
812B
HF VIDEO
1H
GAIN ADJ.
ADD TO 262 LINE COMB
810
812C
GAIN ADJ.
ADD TO 263 LINE COMB
816
812D
GAIN ADJ.
OPTIONAL LINE COMB

FIG. 8